What is claimed is:

1. A method for forming an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less than about 4.0;

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via; and

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method.

2. The method of claim 1 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

3. The method of claim 1 wherein the patterned first dielectric layer and the blanket second dielectric layer are each formed from a separate dielectric material selected from the group consisting of spin-on-polymer (SOP) dielectric materials, spin-on-glass (SOG) dielectric materials, amorphous carbon dielectric materials, diamond like carbon dielectric materials, carbonaceous silicate glass (CSG) dielectric materials, fluorosilicate glass (FSG) dielectric materials and aerogel dielectric materials.

4. The method of claim 1 wherein there is not formed an extrinsic hard mask layer interposed between the patterned first dielectric layer and the blanket second dielectric layer.

5. The method of claim 1 wherein the patterned first dielectric layer is formed to a thickness of from about 4000 to about 10000 angstroms.

6. The method of claim 1 wherein the blanket second dielectric layer is formed to a thickness of from about 4000 to about 7000 angstroms.

7. The method of claim 1 wherein the patterned mask layer is selected from the group consisting of patterned photoresist mask layers and patterned hard mask layers.

8. A method for forming a patterned conductor layer within an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less than about 4.0;

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via;

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method; and

forming within the aperture a contiguous patterned conductor interconnect and patterned conductor stud layer.

9. The method of claim 8 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

10. The method of claim 8 wherein the patterned first dielectric layer and the blanket second dielectric layer are each formed from a separate dielectric material selected from the group consisting of spin-on-polymer (SOP) dielectric materials, spin-on-glass (SOG) dielectric materials, amorphous carbon dielectric materials, diamond like carbon dielectric materials, carbonaceous silicate glass (CSG) dielectric materials, fluorosilicate glass (FSG) dielectric materials and aerogel dielectric materials.

11. The method of claim 8 wherein there is not formed an extrinsic hard mask layer interposed between the patterned first dielectric layer and the blanket second dielectric layer.

12. The method of claim 8 wherein the patterned first dielectric layer is formed to a thickness of from about 4000 to about 10000 angstroms.

13. The method of claim 8 wherein the blanket second dielectric layer is formed to a thickness of from about 4000 to about 7000 angstroms.

14. The method of claim 8 wherein the patterned mask layer is selected from the group consisting of patterned photoresist mask layers and patterned hard mask layers.

15. The method of claim 8 wherein the contiguous patterned conductor interconnect and patterned conductor stud layer is formed within the aperture while employing a chemical mechanical polish (CMP) planarizing method.